CLAIMS

Sub B1 >

1. A power on reset circuit, comprising:

a. a first circuit for applying a first voltage to said power on reset circuit;

b. a circuit for starting a phase locked loop when voltage applied by said first circuit exceeds a threshold and for inhibiting operation of at least a plurality of clocks until released, and

c. releasing all inhibited clocks once voltage stability is achieved.

2. The power on reset circuit of claim 1 further comprising a switched converter in which the duty cycle of said switched converter is unity until the output of said switched converter reaches substantially said first voltage.

3. The power on reset circuit of claim 2 in which the duty cycle of said switched converter is programmable.

4. The power on reset circuit of claim 3 in which the duty cycle of said switched converter is reduced from unity after the output of said switched converter reaches substantially said first voltage.

5. The power on reset circuit of claim 3 in which said switched converter settles to a set output voltage before said inhibited clocks are released.

6. The power on reset circuit of claim 1 further comprising a regulator and in which the inhibited clocks are released only after said regulator substantially reaches its stabilized output voltage.

7. The power on reset circuit of claim 1 contained within an integrated circuit.

8. A method of applying power to an integrated circuit, comprising the steps of:

a. applying a first voltage to said integrated circuit;

b. when voltage applied to said integrated circuit exceeds a first threshold, setting the duty cycle of a switched converter to substantially unity and placing a hold on the operation of at least one clock on said integrated circuit;

c. allowing a phase locked loop to start; and

d. when the output of the switched converter nears said first voltage, reducing the duty cycle of said switched converter; and

e. after the output of the switched converter reaches stability, releasing said hold.

9. The method of claim 8 in which the hold on more than one clock is released in stages.

10. The method of claim 8 in which said switched converter is programmable over a bus.

11. The method of claim 10 in which said switched converter is programmable over a communications link exterior to said integrated circuit.

12. A method of applying power to an integrated circuit, comprising the steps of:

a. applying a first voltage to said integrated circuit;

b. when voltage applied to said integrated circuit exceeds a first threshold placing a hold on the operation

of at least one clock on said integrated circuit and allowing a phase locked loop to start; and

c. when the output of a regulator reaches stability, releasing said hold.

13. The method of claim 11 in which the hold on more than one clock is released in stages.

14. A program product, comprising:

a. a memory medium; and

b. control instructions stored on said memory medium, said control instructions causing application of a first voltage to an integrated circuit, when voltage applied to said integrated circuit exceeds a first threshold, setting a duty cycle of a switched converter to substantially unity and placing a hold on the operation of at least one clock on said integrated circuit, allowing a phase locked loop to start; and when the output of the switched converter nears said first voltage, reducing the duty cycle of said switched converter; and after the output of the switched converter reaches stability, releasing said hold.

15. The program product of claim 14 in which said hold is released in stages.

16. A program product, comprising;

a. a memory medium; and

b. control instructions stored on said memory medium, said control instructions causing application of a first voltage to said integrated circuit, when voltage applied to said integrated circuit exceeds a first threshold placing a hold on the operation of at least one clock on said integrated circuit and allowing a phase locked loop to start; and when the output of a regulator reaches stability, releasing said hold.

17. The program product of claim 16 in which said hold is released in stages.